AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) A chip-level architecture comprising:

a monolithic three-dimensional write-once memory array, wherein the monolithic three-dimensional write-once memory array comprises:

a first conductor;

a first memory cell above the first conductor;

a second conductor above the first memory cell; and

a second memory cell above the second conductor;

wherein the second conductor is the only conductor between the first and second memory cells; and

at least two of the following system blocks:

an Error Checking & Correction Circuit (ECC);

a Checkerboard Memory Array containing sub arrays;

a Write Controller;

a Charge Pump;

a Vread Generator;

an Oscillator;

a Band Gap Reference Generator; and

a Page Register/Fault Memory.

2. (Original) The invention of Claim 1, further comprising a third system block.

3. (Original) The invention of Claim 1, wherein one of the system blocks is the Vread Generator.

4. (Original) The invention of Claim 3, wherein the Vread Generator provides a voltage to which a selected word line is driven during a read operation.

5. (Original) The invention of Claim 4, wherein two control transistors per group of memory sub arrays are spatially distributed throughout the die to achieve reduced voltage drop along reference node Vread.

6. (Original) The invention of Claim 1, wherein one of the system blocks is the write controller, and wherein groups of selected sub arrays are connected together by bidirectional data lines and are connected to the write controller.

7. (Original) The invention of Claim 6, wherein selected cells are in selected sub arrays, each of which has a coordinated row decoder for locating the selected cells.

8. (Original) The invention of Claim 1, wherein one of the system blocks is the write controller, and further comprising a fault memory and a logic block, wherein entries in the fault

memory are determined by the write controller during the write operation and read by the logic block to activate a write operation to a redundant row.

9. (Original) The invention of Claim 6, wherein the connection between the groups of sub arrays and the write controller includes data lines and control lines, said lines which are at least partially formed on a level of wiring at or near a top surface of the memory array.

10. (Original) The invention of Claim 9 wherein the data and control lines are substantially parallel to memory array lines used for sensing data in memory cells.

11. (Original) The invention of Claim 6, wherein the selected sub arrays contain user data cells, ECC data cells and cells containing redundancy control bits.

Claims 12-20 (Withdrawn)

21. (Currently Amended) A chip-level architecture comprising:

a monolithic three-dimensional write-once memory array, wherein the monolithic three-dimensional write-once memory array comprises:

a first conductor;

a first memory cell above the first conductor;

a second conductor above the first memory cell; and

a second memory cell above the second conductor;

wherein the second conductor is the only conductor between the first and second memory cells;

ECC; and

smart write.

Claims 22-28 (Withdrawn)

Claims 29 and 30 (Cancelled)

31. (New) The invention of Claim 1, wherein the first memory cell, second memory cell, and second conductor are all in a plane defined by the second conductor, and wherein the second conductor is the only conductor between the first and second memory cells in the plane.

32. (New) The invention of Claim 21, wherein the first memory cell, second memory cell, and second conductor are all in a plane defined by the second conductor, and wherein the second conductor is the only conductor between the first and second memory cells in the plane.